

# PCIE16X-402EVK User Guide

## PCle 16X Lane Card Evaluation Kit

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### General Description:

The PCIE16X-402EVK is a PCIe add-in riser card for PCIe 16x applications. It provides a complete platform to evaluate 4 - DS80PCI402SQ, 4 Lane PCIe repeaters for PCIe system protocol and lane negotiation validation. The card has a 16X PCIe edge fingers at J1 which plugs into a motherboard that has a PCIe 16X connector. The card also has a PCIe 16X connector at J2 for endpoint connection (PCIe graphic card or SATA/SAS raid controller card).

### Features:

- 8 channel PCIe repeater up to 8 Gbps (GEN 3)
- Low power consumption, with option to power down unused channels
- Adjustable receive equalization
- Adjustable transmit VOD and De-emphasis
- IDLE detection — squelch function auto mutes the output
- Programmable via pin selection or SMBus interface
- Single supply operation: VIN = 3.3V±10% or VDD = 2.5V ±5%
- -40°C to +85°C Operation
- >6 kV HBM ESD Rating
- High speed signal flow-thru pin-out package - SQA54A: 54-pin LLP (10 mm x 5.5 mm, 0.5 mm pitch)

### Applications:

- Extends FR-4 Backplane Trace for PCIe Applications

### PCIE16X-402EVK Demo Kit Contents:

- End User License Agreement
- PCIE16X-402EVK User Guide Rev 1.2
- PCIE16X-402EVK Board

### Ordering Information:

**DEVICE:** DS80PCI402SQE: QTY = 250, DS80PCI402SQ: QTY = 2,000

**SMA Evaluation Kit:** PCIE16X-402EVK



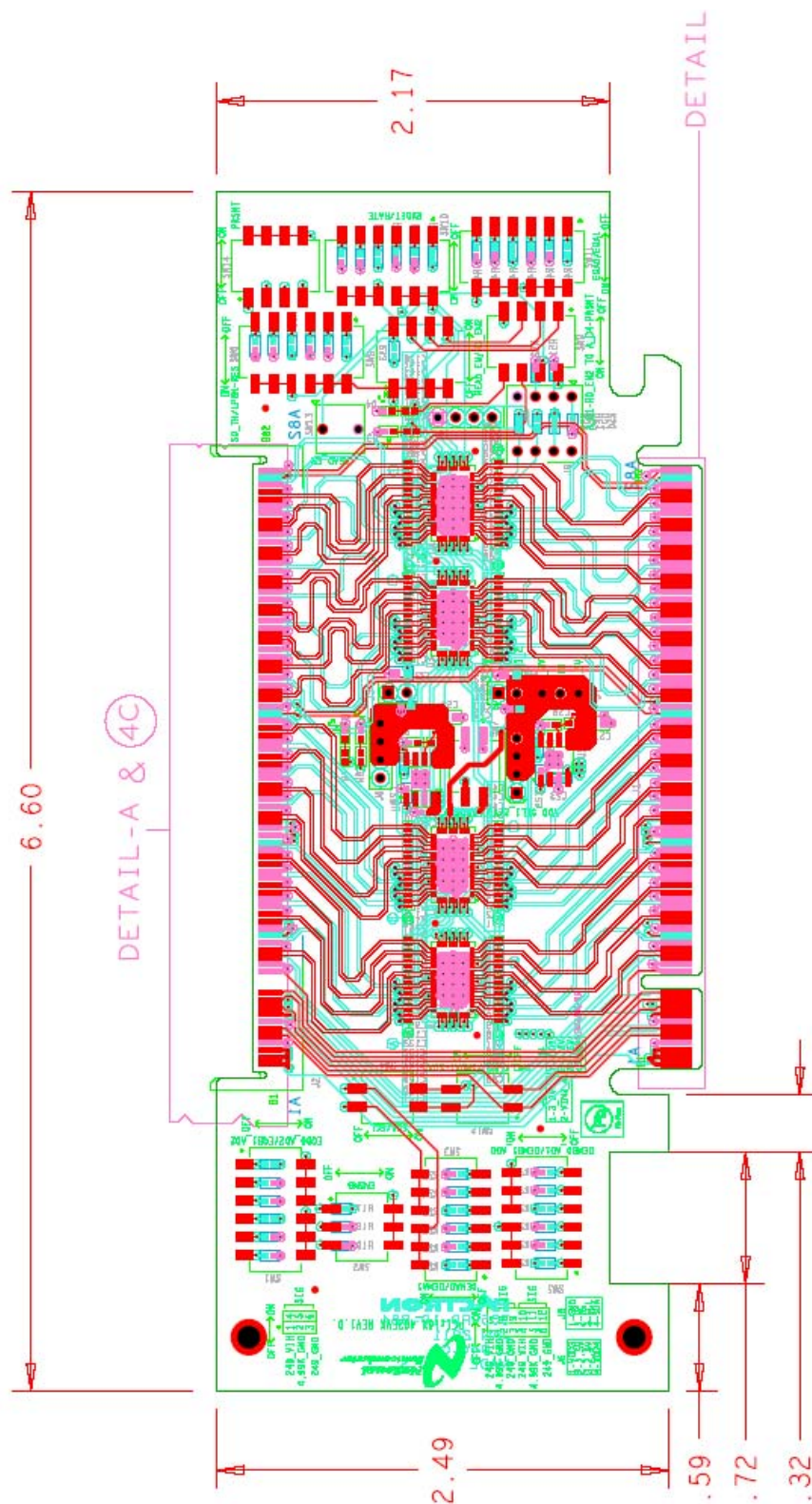


Figure 1. PCIE16X-402EVK Evaluation Board

**Table 1. Switches to set the 4-level input control pins**

<b>4 – level Input Settings</b>	<b>Setting for 3 pin switches (3-2-1)</b>
0 – Tie 249 ohm to GND	<b>ON</b> – OFF – OFF
R – Tie 5k ohm to GND	OFF – <b>ON</b> – OFF
F – FLOAT (open)	OFF – OFF – OFF
1 – Tie 249 ohm to VIH	OFF – OFF – <b>ON</b>

The following switches are used to set the input condition for the 4-level inputs:

SW1, SW2, SW3, SW5, SW6, SW10, SW11.

There are 3 switches connected to an input signal pin. Each switch when set to the ON position sets the pin to one of the 4-level setting. The 6 pin switches are assigned similar to the 3 pin switches. The only difference is 2 signal pins are connected and thus 6-5-4 is for the one signal pin and 3-2-1 is for another signal pin. Please note only 1 switch at the ON position is allowed.

**Table 2. Connection and Control Description**

<b>Component</b>	<b>Name</b>	<b>Function</b>
J1	PCIE TX/RX	High speed differential TX/RX from/to Root Complex
J2	PCIE TX/RX	High speed differential TX/RX to/from End Point
J3, J5	3.3V to VIN	3.3V DC Power – VIN to DS80PCI800SQ Jumper ON = 3.3V mode operation Jumper OFF = 2.5V mode operation
J4, J6	2.5V to VDD	2.5V DC Power – VDD to DS80PCI800SQ Jumper ON (1-2, 3-4) = 2.5V mode operation Jumper OFF (1-2, 3-4) = 3.3V mode operation
J7	VIN or VDD	Jumper VIH: set 1-2 = VIN (3.3V) or set 2-3 = VDD (2.5V)
J8	SDA, SCL	Optional SMBUS access pins. See the datasheet for additional information on SMBUS.
J9	EEPROM	Optional socket for EEPROM
SW1	EQB[1:0] or AD[3:2]	PIN MODE – EQ control for channel B inputs SMBUS MODE – AD[3:2] device address bits
SW2	ENSMB	ENSMB = LOW – PIN MODE ENSMB = HIGH – SMBUS (slave mode) ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM)
SW3	DEMA[1:0]	PIN MODE – DE control for channel A outputs
SW4	SDA/SCL	“ON” position connects SDA and SCL lines to the device pin.
SW5	DEMB[1:0] or AD[1:0]	PIN MODE – DE control for channel B outputs SMBUS MODE – AD[1:0] device address bits
SW6	SD_TH and LPBK – RES	SD_TH – Signal detect threshold level (FLOAT = Default level) LPBK function for PCI402 and RESERVED for PCI800 (FLOAT = Normal operation)
SW7	VDD_SEL1 VDD_SEL2	VDD_SEL – Enable or disable the internal 3.3V to 2.5V regulator for U1 and U2. ON connects to GND to enable the internal LDO regulator for 3.3V mode operation.
SW8	READ_EN, RD_EN2, RD_EN3 and RD_EN4	For manual control of loading the external EEPROM and daisy chain the READ_EN to the ALL_DONE pins. Pin1 = ON connects the SW13 push button to the READ_EN of U1. Pin2,3,4 = OFF
SW9	A_D1 to RD_EN2 ... A_D3 to RD_EN4	Pin1 = ON connects the ALL_DONE of U1 to READ_EN of U2. Pin2 = ON connects the ALL_DONE of U2 to READ_EN of U3. Pin3 = ON connects the ALL_DONE of U3 to READ_EN of U4. Pin4 = OFF
SW10	RXDET and RATE	RXDET – Input internal 50 ohm to VDD terminations RXDET = F (AUTO RX Detect), RXDET = 1 (50 ohm input termination). RATE = 0 (GEN1,2) = 2.5G / 5.0G. RATE = R (GEN3) = 8.0G. RATE = F (AUTO Detect). The RATE auto detect circuit requires the idle and active signal which occurs during the link training negotiation.
SW11	EQA[1:0]	PIN MODE – EQ control for channel A inputs

SW12	SDA/SCL to SMCLK/SMDAT	"ON" connect the SDA/SCL bus to the PCIe SMCLK and SMDAT bus. Default is "OFF".
SW13	READ_EN	ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM) SW6: SD_TH becomes the READ_EN pin. To start the loading at power up, set SW6 pin 3 to "ON" position (pull to GND). To manually control the start, set SW6 to "OFF" position and set SW8 pin1 to "ON" and pin2 to "OFF" position and push the SW13 button for the high to low transition to start the loading. When the loading is complete the LEDs – D1 and D2 light should turn OFF.
SW14	PRSNT	"ON" connects the PCIe PRSNT signal to the device PRSNT pin. For 16X, set all the switches to the "ON" position.

## Quick Start User Guide:

1. Connect J1 – PCIe 16x edge finger to the motherboard (root complex)
2. Connect J2 - PCIe 16x connector to an add-in card (end point).
3. For 3.3V mode operation, set J3 jumper to ON and do not use J4 (leave jumper OFF).  
For 2.5V mode operation, set J3 jumper to OFF and set J4 jumper to ON (1-2 and 3-4).
4. Set jumper – J7 for VIH connection to VIN (3.3V) or VDD (2.5V). Default is 1-2 set to ON for VIH = 3.3V.
5. Set SW7 – VDD\_SEL1\_2 and VDD\_SEL3\_4 to "ON" position for 3.3V mode operation.
6. Set the control pins for normal operation
  - SW10 – RXDET = F (continuous receiver detection): set switches (3-2-1) = (OFF-OFF-OFF).  
RXDET = 1 (50 ohm input termination): set switches (3-2-1) = (OFF-OFF-**ON**).
  - SW10 – RATE = F (enable rate detection): set switches (6-5-4) to (OFF-OFF-OFF).  
RATE = R (GEN3 mode): set switches (6-5-4) = (OFF-**ON**-OFF).  
RATE = 0 (GEN1,2 mode): set switches (6-5-4) = (**ON**-OFF-OFF).
  - SW6 – SD\_TH = F (default signal detect threshold level): set switches (3-2-1) = (OFF-OFF-OFF).
  - SW6 – LPBK - RES = F (normal operation): set switches (6-5-4) = (OFF-OFF-OFF).
  - SW8: Set switches to "OFF" position.
  - SW9: Set switches to "OFF" position.
  - SW14 – PRSNT = GND (enables the device): set switches to "ON" position.

### 5. Set the input equalization level.

For external pin mode control of the equalization level:  
Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).  
SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.  
Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:

Set EQB[1:0] with SW1 for the B bank of inputs (top 2 left inputs of DS80PCI402).  
SW1 (6-5-4), (3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQB[1:0] = R,R = 14.6 dB at 4 GHz (level 6).  
Set EQA[1:0] with SW11 for the A bank of inputs (bottom 2 left inputs of DS80PCI402).  
SW8 (6-5-4), (3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQA[1:0] = R,R = 14.6 dB at 4 GHz (level 6).  
The table below is the 16 possible EQ settings.

Level	EQA/B[1:0]	SW1 - EQB[1:0] SW11 - EQA[1:0]						EQ (dB) at 4 GHz
		6	5	4	3	2	1	
1	0, 0	<b>ON</b>	OFF	OFF	<b>ON</b>	OFF	OFF	4.9
2	0, R	<b>ON</b>	OFF	OFF	OFF	<b>ON</b>	OFF	7.9
3	0, F	<b>ON</b>	OFF	OFF	OFF	OFF	OFF	9.9
4	0, 1	<b>ON</b>	OFF	OFF	OFF	OFF	<b>ON</b>	11.0
5	R, 0	OFF	<b>ON</b>	OFF	<b>ON</b>	OFF	OFF	14.3
6	R, R	OFF	<b>ON</b>	OFF	OFF	<b>ON</b>	OFF	14.6
7	R, F	OFF	<b>ON</b>	OFF	OFF	OFF	OFF	17.0



8	R, 1	OFF	<b>ON</b>	OFF	OFF	OFF	<b>ON</b>	18.5
9	F, 0	OFF	OFF	OFF	<b>ON</b>	OFF	OFF	18.0
10	F, R	OFF	OFF	OFF	OFF	<b>ON</b>	OFF	22.0
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	24.4
12	F, 1	OFF	OFF	OFF	OFF	OFF	<b>ON</b>	25.8
13	1, 0	OFF	OFF	<b>ON</b>	<b>ON</b>	OFF	OFF	27.4
14	1, R	OFF	OFF	<b>ON</b>	OFF	<b>ON</b>	OFF	29.0
15	1, F	OFF	OFF	<b>ON</b>	OFF	OFF	OFF	31.4
16	1, 1	OFF	OFF	<b>ON</b>	OFF	OFF	<b>ON</b>	32.7

6. Set the output VOD and De-emphasis level.

**For external pin mode control for the VOD and De-emphasis level:**

Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).

SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.

Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:

Set DEMB[1:0] with SW5 for the B bank of outputs (top 2 right outputs of DS80PCI402).

SW5 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMB[1:0] = 0,1 (VOD=1.0V, DE=0 dB).

Set DEMA[1:0] with SW3 for the A bank of outputs (bottom 2 right outputs of DS80PCI402).

SW3 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMA1:0] = 0,1 (VOD=1.0V, DE=0 dB).

The table below is the 16 possible settings of VOD and DE when in pin mode.

In Gen 1/2, the de-emphasis level can be set with the DEMx[1:0] pins, but is not available in Gen 3.

Level	DEMA/B[1:0]	SW5 - DEMB[1:0] SW3 - DEMA[1:0]						GEN1,2	
		6	5	4	3	2	1	VOD (Vp-p)	DE (dB)
1	0, 0	<b>ON</b>	OFF	OFF	<b>ON</b>	OFF	OFF	0.8	0
2	0, R	<b>ON</b>	OFF	OFF	OFF	<b>ON</b>	OFF	0.9	0
3	0, F	<b>ON</b>	OFF	OFF	OFF	OFF	OFF	0.9	-3.5
4	0, 1	<b>ON</b>	OFF	OFF	OFF	OFF	<b>ON</b>	1.0	0
5	R, 0	OFF	<b>ON</b>	OFF	<b>ON</b>	OFF	OFF	1.0	-3.5
6	R, R	OFF	<b>ON</b>	OFF	OFF	<b>ON</b>	OFF	1.0	-6
7	R, F	OFF	<b>ON</b>	OFF	OFF	OFF	OFF	1.1	0
8	R, 1	OFF	<b>ON</b>	OFF	OFF	OFF	<b>ON</b>	1.1	-3.5
9	F, 0	OFF	OFF	OFF	<b>ON</b>	OFF	OFF	1.1	-6
10	F, R	OFF	OFF	OFF	OFF	<b>ON</b>	OFF	1.2	0
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	1.2	-3.5
12	F, 1	OFF	OFF	OFF	OFF	OFF	<b>ON</b>	1.2	-6
13	1, 0	OFF	OFF	<b>ON</b>	<b>ON</b>	OFF	OFF	1.3	0
14	1, R	OFF	OFF	<b>ON</b>	OFF	<b>ON</b>	OFF	1.3	-3.5
15	1, F	OFF	OFF	<b>ON</b>	OFF	OFF	OFF	1.3	-6
16	1, 1	OFF	OFF	<b>ON</b>	OFF	OFF	<b>ON</b>	1.3	-9

**For SMBUS mode control of the EQ, VOD and De-emphasis level:**

Set ENSMB = 1 (1kohm to VIH) by using the SW2 (3-2-1) = (OFF-OFF-**ON**).

Set SW4 pin1,2 to the ON position so the SMBUS signals are connected.

Set SW3 pin1 thru pin6 switches to the OFF position so they do not connect to the SDA and SCL line.

Set the SW1 and SW5 for the AD[3:0] pins. AD[3:0]=0000 sets device slave address = B0'hex.

Connect SDA, SCL and GND to J17. Please refer to datasheet for register map for EQ, VOD and DEM.



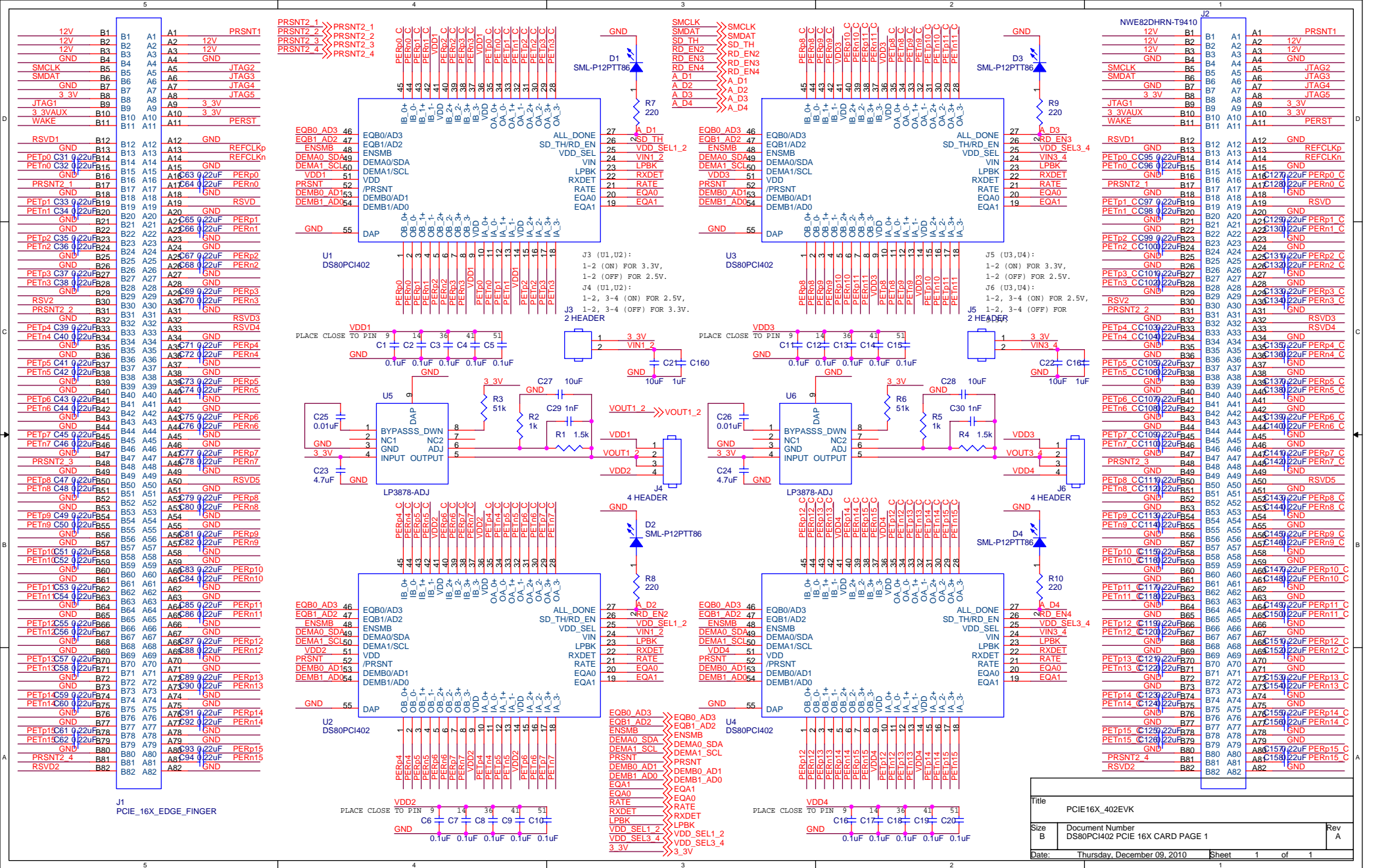
## Bill of Materials for PCIE16X\_402EVK:

Item	Qty	Reference	Digikey PN	Manufacture PN	Descriptions
1	20	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20	445-4711-1-ND	C0603X5R0J104M	CAP CER .10UF 6.3V X5R 0201
2	4	C21,C22,C27,C28	445-3448-1-ND	C1608Y5V0J106Z	CAP CER 10UF 6.3V Y5V 0603
3	2	C23,C24	587-1966-1-ND	AMK105BJ475MV-F	CAP CER 4.7UF 4V X5R 0402
4	2	C25,C26	445-5515-1-ND	C0402X5R0J103K	CAP CER 0.01UF 6.3V X5R 01005
5	2	C29,C30	490-1261-1-ND	GRM033R71C102KD01D	CAP CER 1000PF 16V 10% X7R 0201
6	2	C160,C161	445-4998-1-ND	C1005X5R0J105K	CAP CER 1.0UF 6.3V X5R 0402
7	128	C31,C32,C33,C34,C35,C36, C37,C38,C39,C40,C41,C42, C43,C44,C45,C46,C47,C48, C49,C50,C51,C52,C53,C54, C55,C56,C57,C58,C59,C60, C61,C62,C63,C64,C65,C66, C67,C68,C69,C70,C71,C72, C73,C74,C75,C76,C77,C78, C79,C80,C81,C82,C83,C84, C85,C86,C87,C88,C89,C90, C91,C92,C93,C94,C95,C96, C97,C98,C99,C100,C101, C102,C103,C104,C105,C106, C107,C108,C109,C110,C111, C112,C113,C114,C115,C116, C117,C118,C119,C120,C121, C122,C123,C124,C125,C126, C127,C128,C129,C130,C131, C132,C133,C134,C135,C136, C137,C138,C139,C140,C141, C142,C143,C144,C145,C146, C147,C148,C149,C150,C151, C152,C153,C154,C155,C156, C157,C158	587-2483-1-ND	LMK063BJ224MP-F	CAP CER .22UF 10V X5R 20% 0201
8	4	D1,D2,D3,D4	511-1592-1-ND	SML-P12PTT86	LED GREEN 0.2MM 13MCD 0402 SMD
9		J1	NA	NA	PCIE EDGE FINGERS
10	1	J2	S2806-ND	NWE82DHRN-T9410	CONN PCI EXPRESS 164POS VERT PCB
11	2	J3, J5	WM6502-ND	22-28-4023	CONN HEADER 2POS .100 VERT GOLD
12	1	J7	WM6503-ND	22-28-4033	CONN HEADER 3POS .100 VERT GOLD
13	3	J4,J6,J8	WM6504-ND	22-28-4043	CONN HEADER 4POS .100 VERT GOLD
14	1	J9	3M5473-ND	4808-3004-CP	SOCKET IC OPEN FRAME 8POS .3"

15	2	R1,R4	P1.50KLCT-ND	ERJ-2RKF1501X	RES 1.50K OHM 1/10W 1% 0402 SMD
16	7	R2,R5,R50,R51,R52,R53, R54	P1.00KLCT-ND	ERJ-2RKF1001X	RES 1.00K OHM 1/10W 1% 0402 SMD
17	2	R3, R6	P51.0KLCT-ND	ERJ-2RKF5102X	RES 51.0K OHM 1/10W 1% 0402 SMD
18	4	R7,R8,R9,R10	P220LCT-ND	ERJ-2RKF2200X	RES 220 OHM 1/10W 1% 0402 SMD
19	26	R11,R13,R14,R16,R17,R19, R20,R22,R23,R25,R26,R28, R29,R31,R32,R34,R35,R37, R38,R40,R41,R43,R44,R46, R47,R49	P249LCT-ND	ERJ-2RKF2490X	RES 249 OHM 1/10W 1% 0402 SMD
20	13	R12,R15,R18,R21,R24,R27, R30,R33,R36,R39,R42,R45, R48	P4.99KLCT-ND	ERJ-2RKF4991X	RES 4.99K OHM 1/10W 1% 0402 SMD
21	2	R55,R56	P2.00KLCT-ND	ERJ-2RKF2001X	RES 2.00K OHM 1/10W 1% 0402 SMD
22	6	SW1,SW3,SW5,SW6,SW10, SW11	CT2196MST-ND	219-6MST	SWITCH TAPE SEAL 6 POS SMD
23	1	SW2	CT2193MST-ND	219-3MST	SWITCH TAPE SEAL 3 POS SMD
24	3	SW4,SW7,SW12	CT2192MST-ND	219-2MST	SWITCH TAPE SEAL 2 POS SMD
25	3	SW8,SW9,SW14	CT2194MST-ND	219-4MST	SWITCH TAPE SEAL 4 POS SMD
26	1	SW13	P12225SCT-ND	EVQ-21505R	SWITCH LT 6MM 160GF 5MM HEIGHT
27	4	U1,U2,U3,U4	NA	DS80PCI402SQ	PCIE REPEATER
28	2	U5,U6	LP3878MR-ADJCT-ND	LP3878MR-ADJ/NOPB	IC VREG 800MA ADJ 8- PSOP

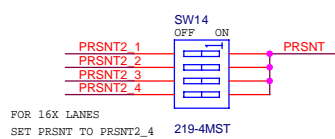
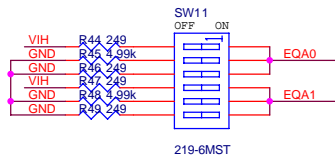
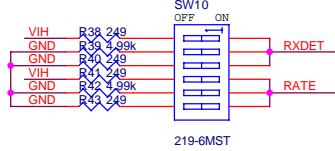
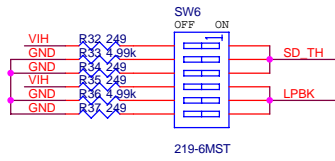
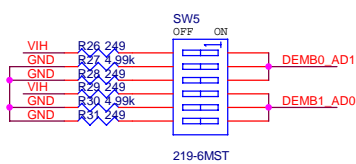
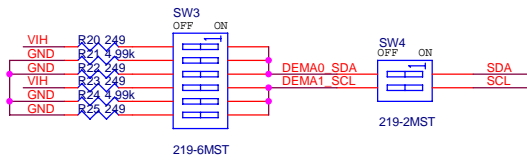
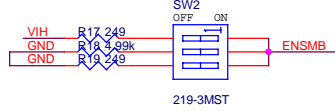
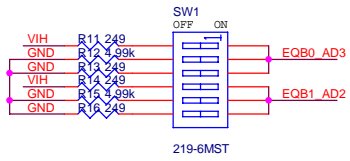




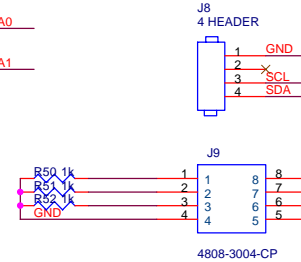
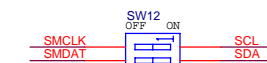
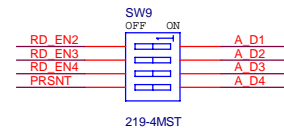
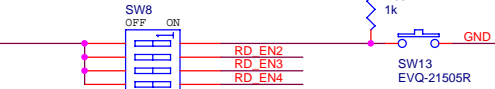
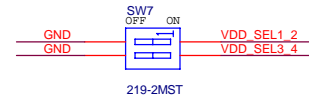




PLACE ALL R<sub>s</sub> CLOSE TO SW  
SW IN THE OFF POSITION = OPEN



FOR 16X LANES  
SET PRNST TO PRNST2\_4



PIN MODE SETTINGS:  
SW1 - EQB0, EQB1  
SW2 - ENSMB = 1K TO GND  
SW3 - DEMA0, DEMA1  
SW4 - OFF POSITION  
SW5 - DEMB0, DEMB1  
SW6 - SD\_TH, LPBK  
SW7 - ON (GND) FOR 3.3V  
SW8 - RD\_EN2-4=ON (SD\_TH)  
SW9 - OFF POSITION  
SW10 - RXDET, RATE  
SW11 - EQA0, EQA1  
SW12 - OFF POSITION  
SW13 - OFF POSITION  
SW14 - PRNST2\_4=ON

SMBUS SLAVE MODE SETTINGS:  
SW1 - AD3, AD2  
SW2 - ENSMB = 1K TO VDD  
SW3 - OFF POSITION  
SW4 - ON POSITION (SDA, SCL)  
SW5 - AD1, AD0  
SW6 - SD\_TH, RES  
SW7 - ON (GND) FOR 3.3V  
SW8 - RD\_EN2-4=ON (SD\_TH)  
SW9 - OFF POSITION  
SW10 - RXDET, RATE  
SW11 - EQA0, EQA1  
SW12 - OFF POSITION WHEN USING SPA BOARD  
SW13 - OFF POSITION  
SW14 - PRNST2\_4=ON

SMBUS MASTER (READ EEPROM) MODE SETTINGS:  
SW1 - AD3, AD2  
SW2 - ENSMB = FLOAT  
SW3 - OFF POSITION  
SW4 - ON POSITION (SDA, SCL)  
SW5 - AD1, AD0  
SW6 - OFF POSITION  
SW7 - ON (GND) FOR 3.3V  
SW8 - SD\_TH=ON, RD\_EN2-4=OFF  
SW9 - ON POSITION (ALL\_DONE TO RD\_EN, ALL\_DONE4 TO PRNST)  
SW10 - RXDET, RATE  
SW11 - EQA0, EQA1  
SW12 - OFF POSITION  
SW13 - GND TO START THE READ PROCESS  
SW14 - OFF POSITION

Title		
PCIE 16X_402EVK		
Size B	Document Number DS80PCI402 PCIE 16X CARD PAGE 2	Rev A
Date:	Thursday, January 06, 2011	Sheet 1 of 1